Models development of new cells protection for electrostatic discharges integrated in Smart Power technology

In collaboration with:

Alma Mater Studiorum – University of Bologna
ARCES (Advanced Research Center on Electronic System)

EIT4SEMM XXXVI cycle- PHD student yearly assessment

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Advisor: Prof. Susanna Reggiani
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State of art:

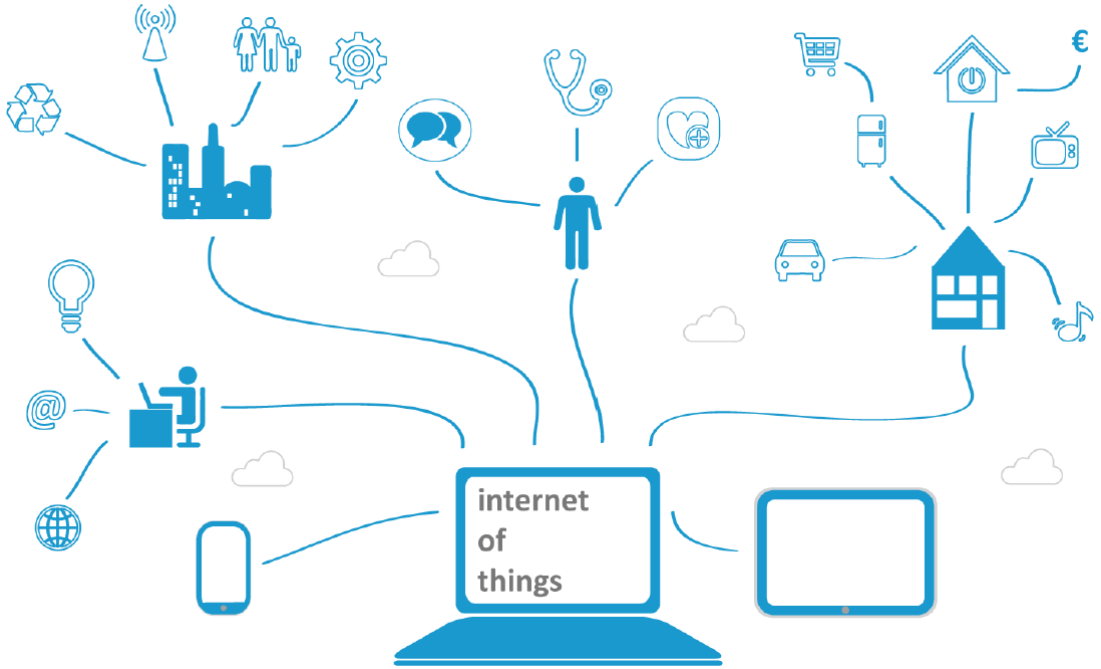
On-chip ESD protection for Internet of Things (IoT)

- 50 billion devices connected to internet
- Endless possibilities in combining

➢ Sensors

➢ Actuators

➢ Networked intelligence



- Productivity (Automotive industries, Manufacturing, retail enviroments , lofistics and navigation)
- Save resources (Cities, homes,)
- Prevent health issues (human, worksites, transportations, factories)

Many of the applications in IoT **require non-standard on-chip ESD protection clamps**

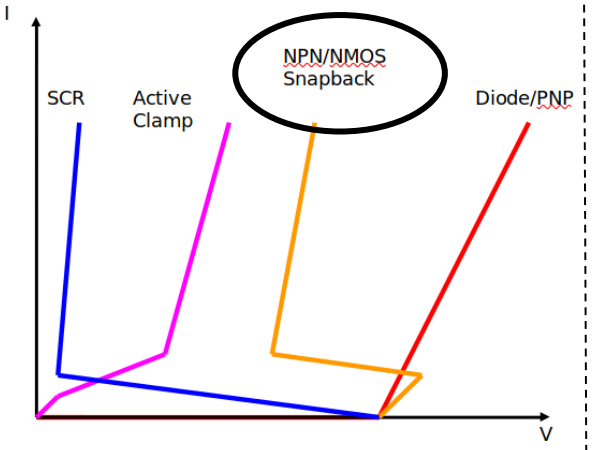
Goal

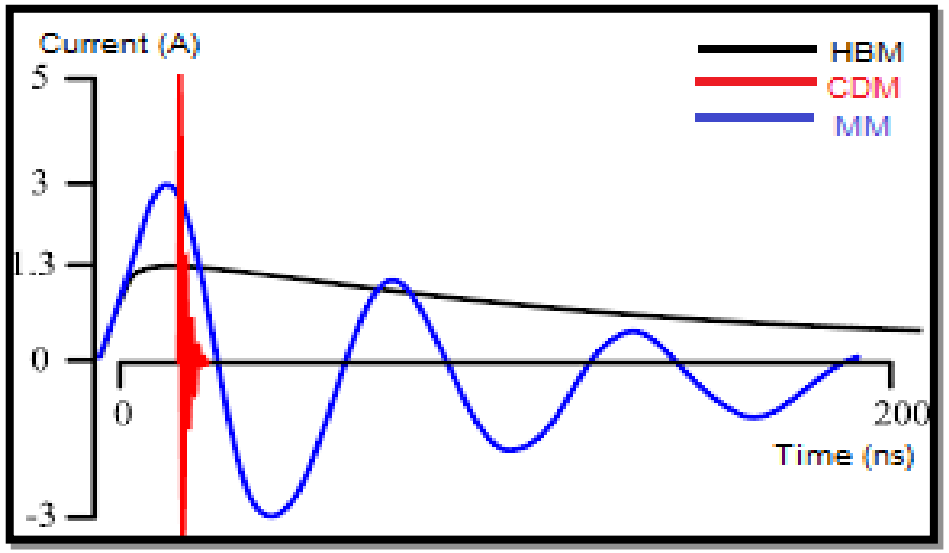
Simulate different possible stress tests over the original ESD protection under test

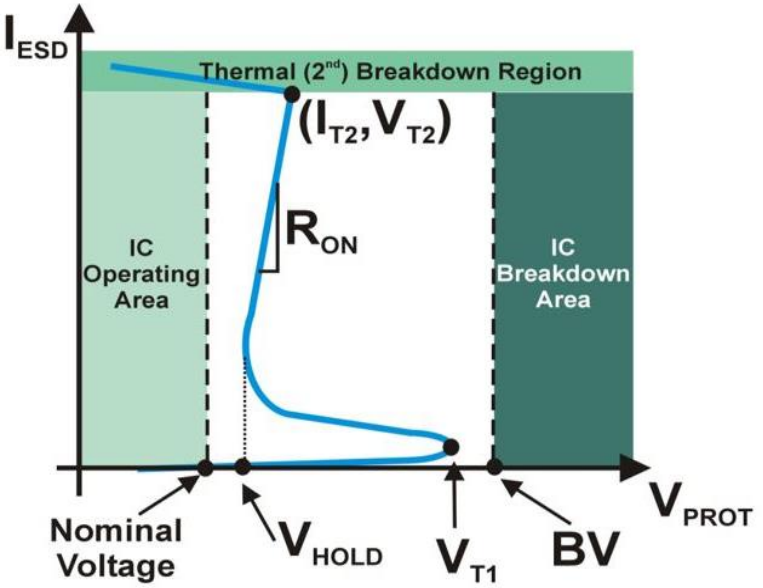
Summary

- Background knowledge
- From layout to TCAD (Technology Computer Aided Design)
- TLP (Transmission Line Pulse) characterization
- Power to failure:
  - Test
  - How to improve performances
- Conclusions

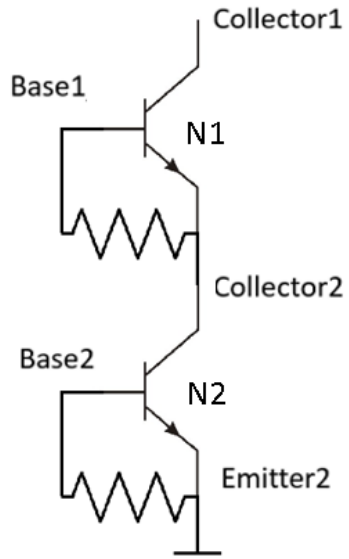
Background Knowledge – ESD common clamps vs. Bipolar transistors under ESD conditions



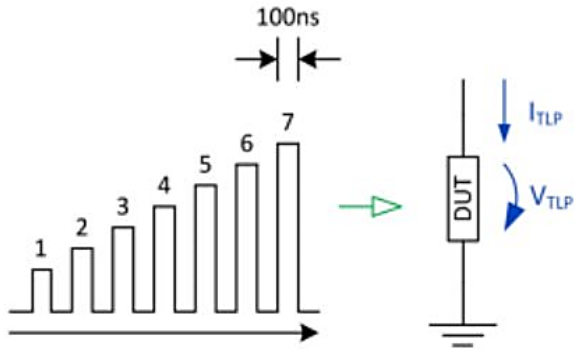




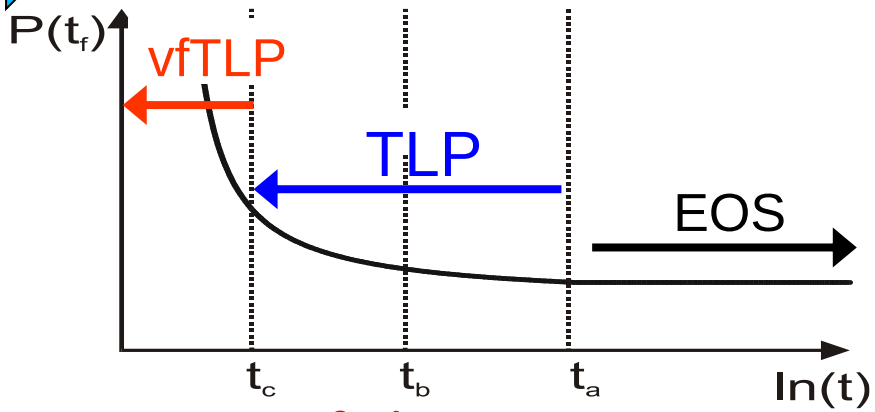
I-V curve reconstructed



DUT



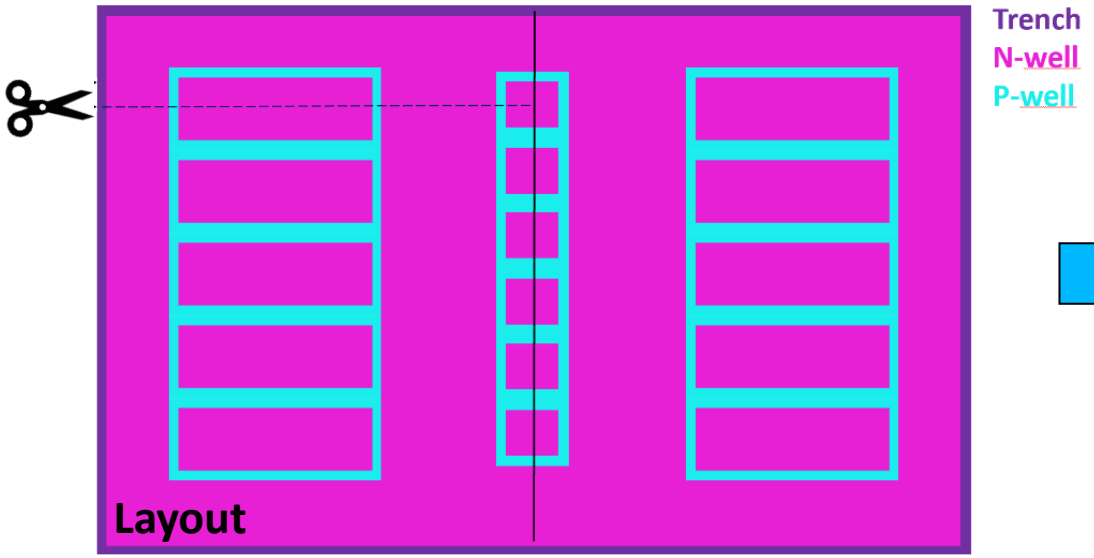
Stress pulses to be modeled

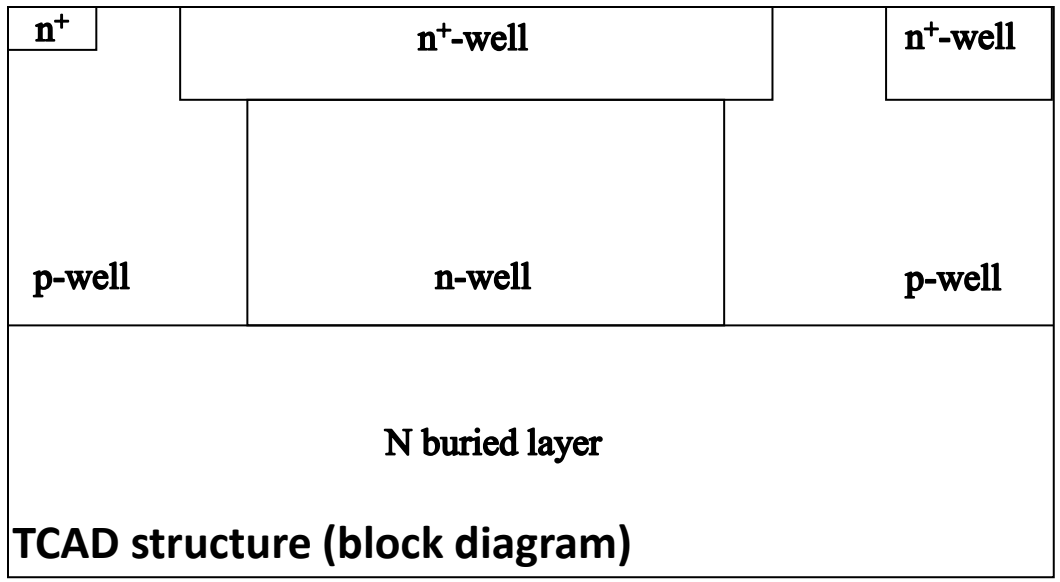


Power- to – failure vs. stress time

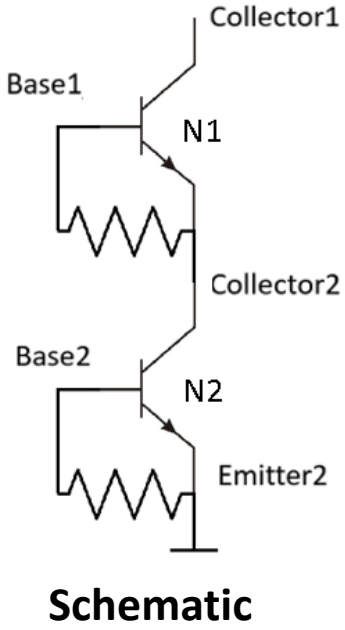
C. Duvvury e A. Amerasekera, ESD in Silicon Integrated Circuits, John Wiley & Sons, LTD, 2002

From layout to TCAD (Technology Computer Aided Design)

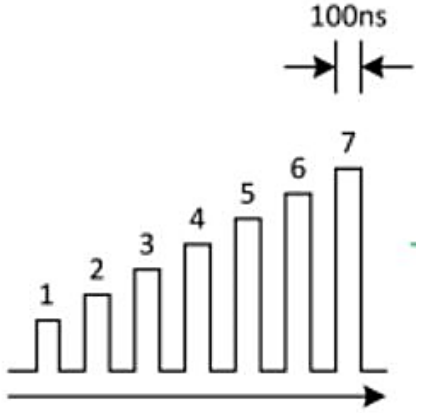




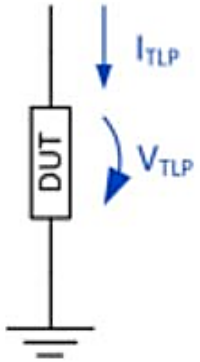
- **Layout structure**:
  - Symmetric with respect to the center
  - BiCMOS technology implementation
- **TCAD structure**:
  - 2D structure sufficient according to layout dimensions
  - Doping profiles tuned with the device fabrication process
  - Selected Physical models to implement impact ionization and thermodynamic behavior of the device



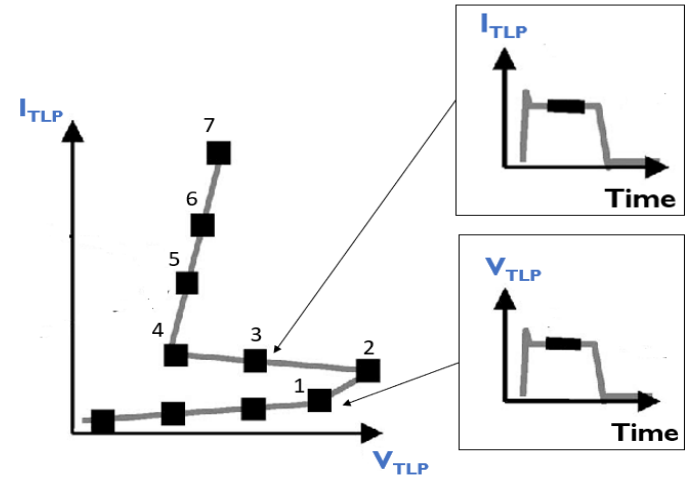
TLP (Transmission Line Pulse) characterization



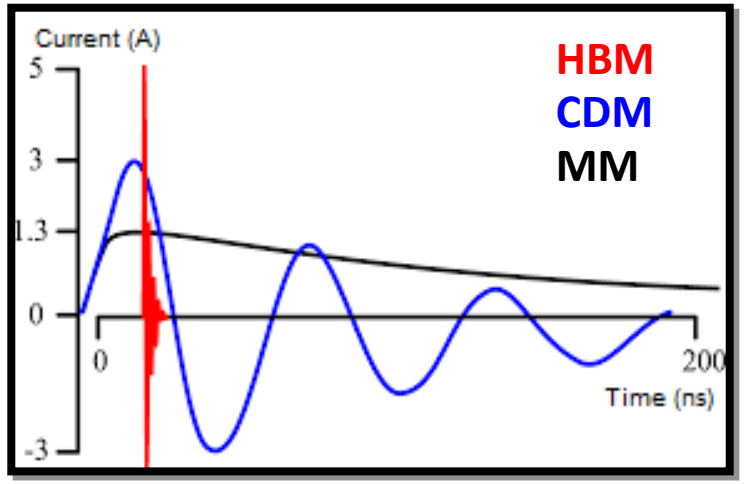
Step 1



Step 2

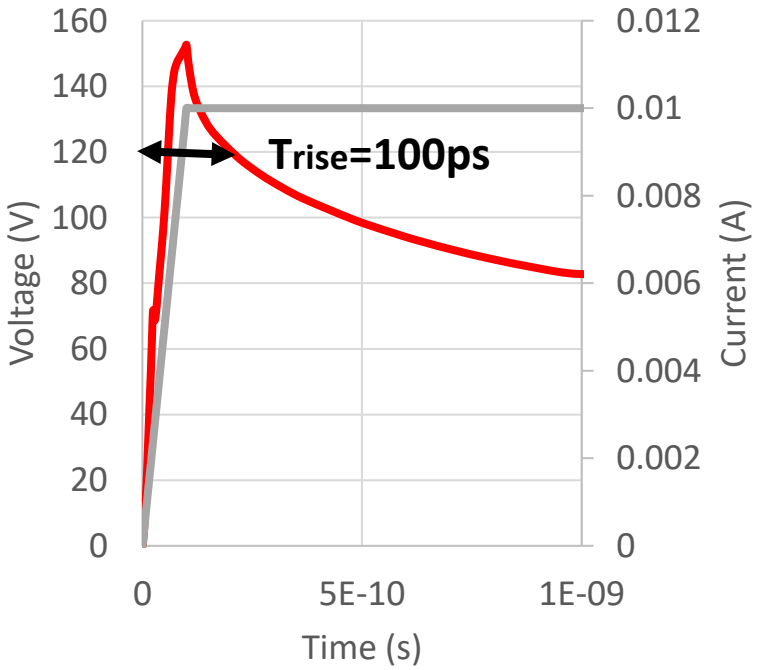


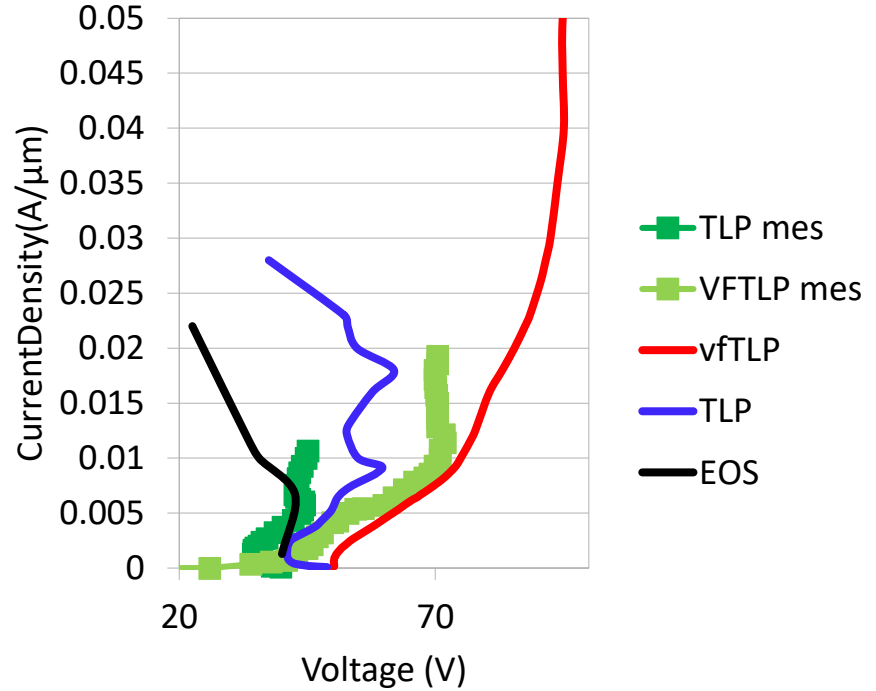
I-V curve reconstruction



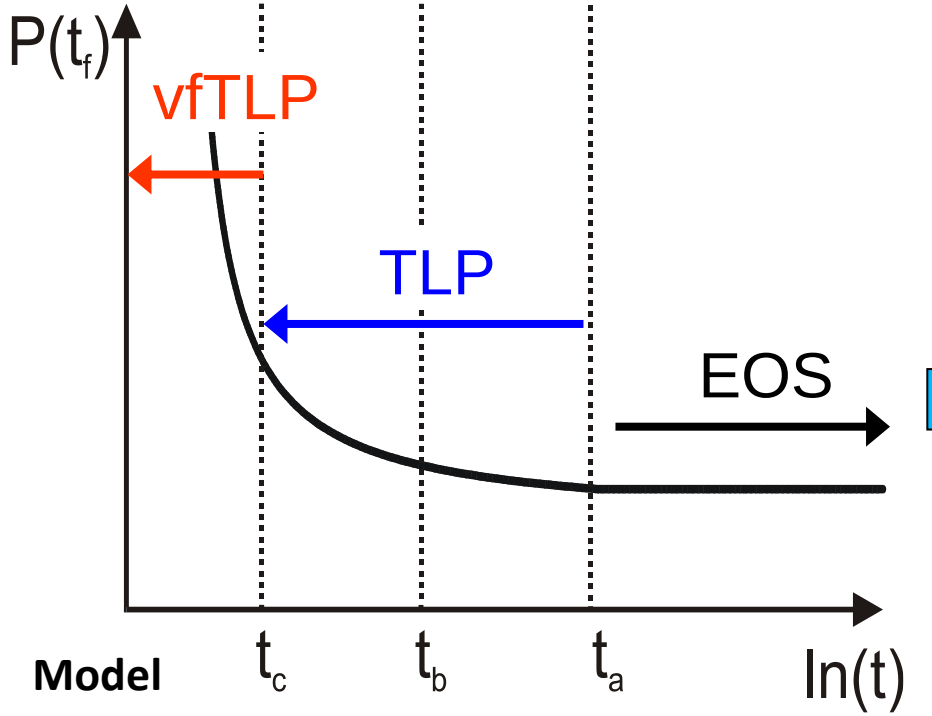
- **HBM: very fast TLP (T_{pulse}=1ns)**
- **CDM: TLP (T_{pulse}=100ns)**
- **MM: EOS (T_{pulse}=500ns)**

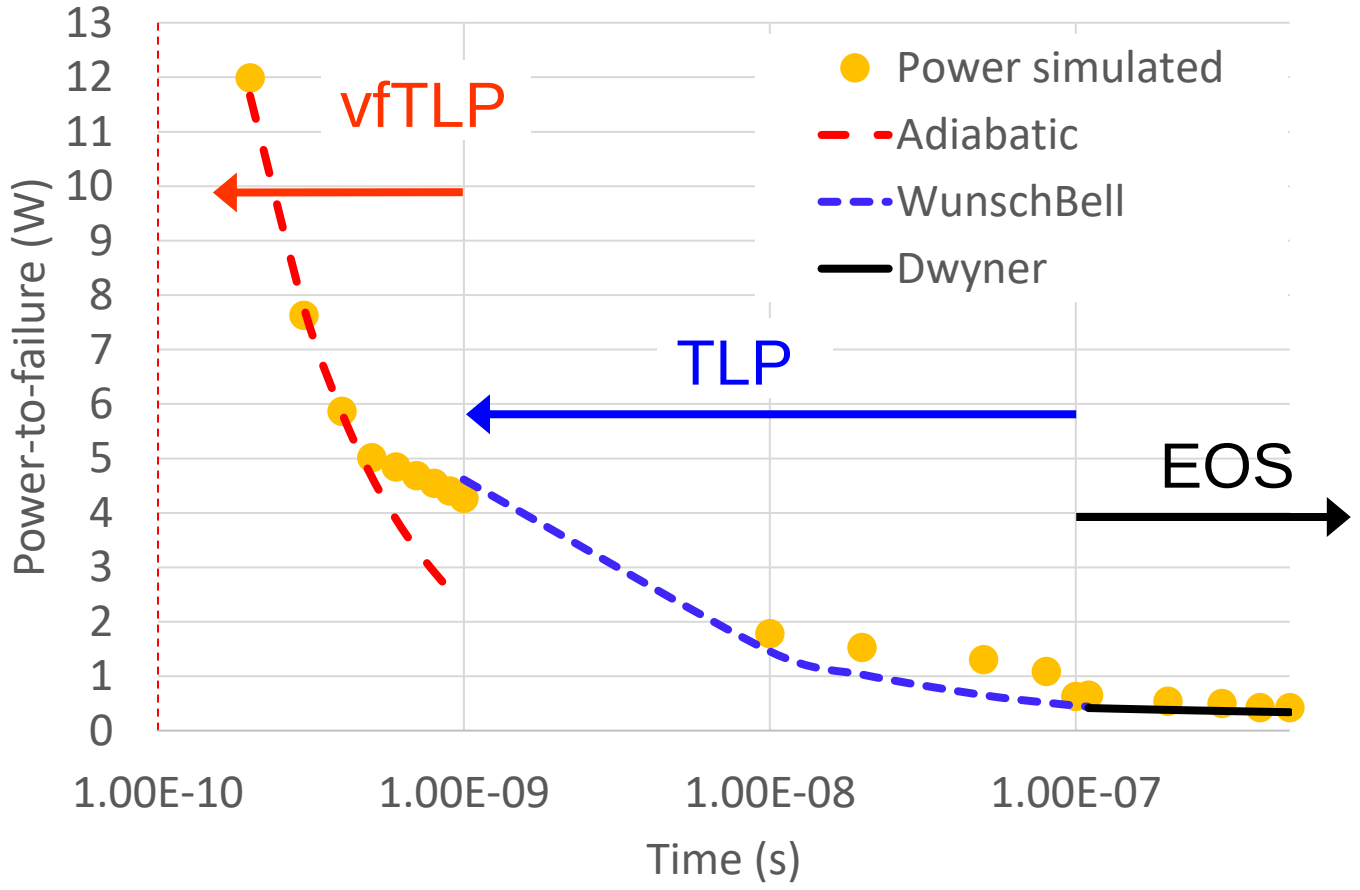
vfTLP





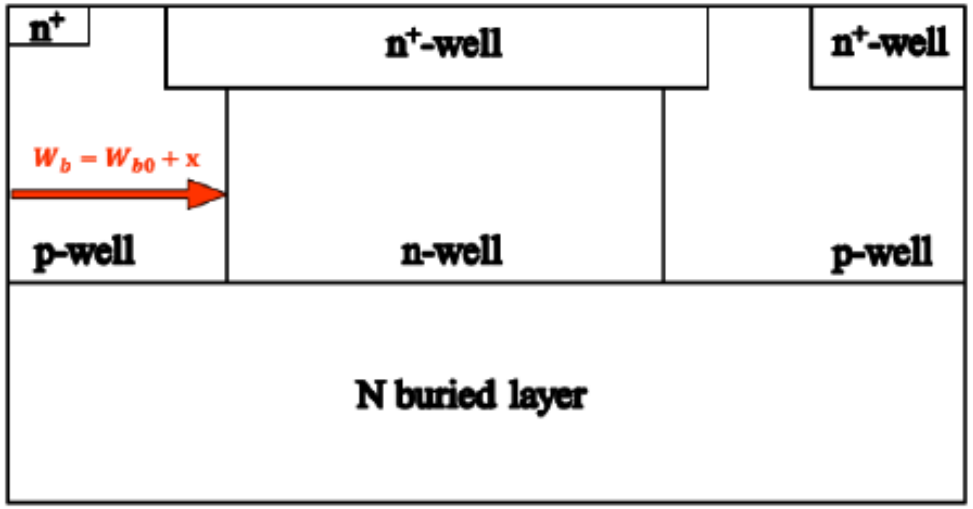
Power – to – Failure test

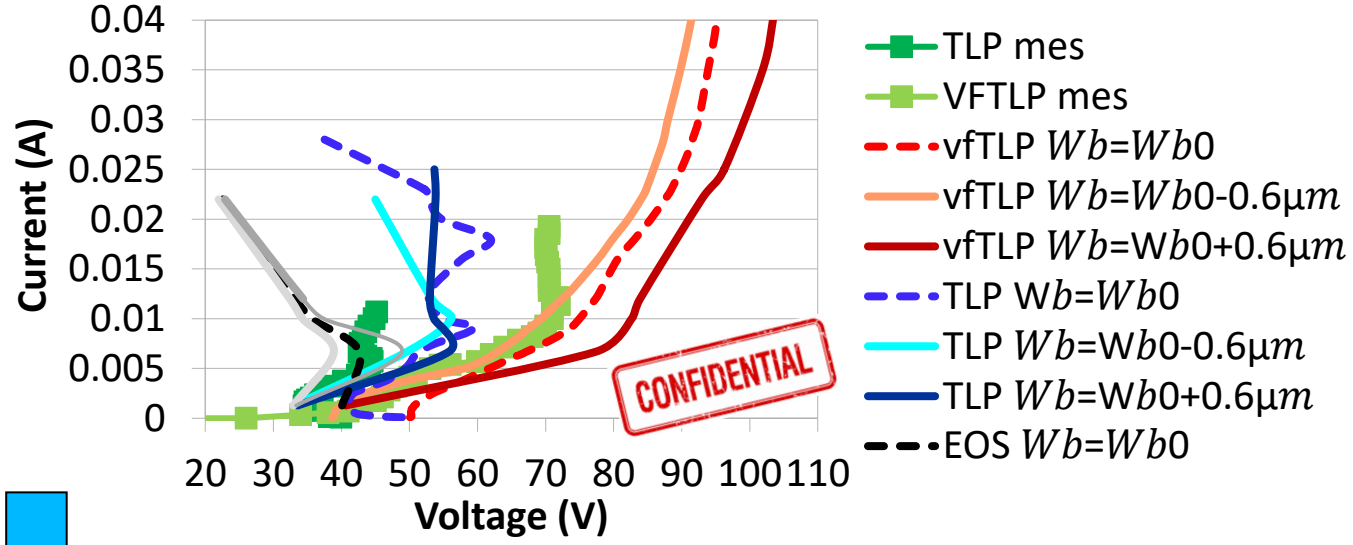


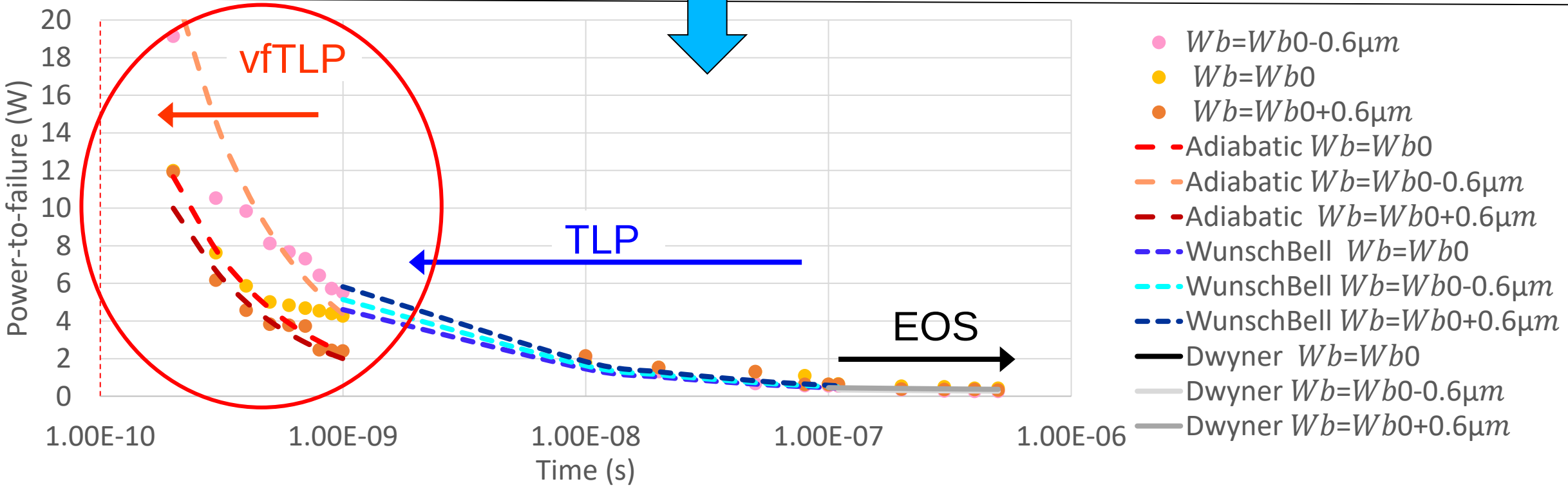


- **$Power_{Failure}$ (t_f)= $I_{failure}$ * $V_{failure}$**
  - $I_{failure}$ and $V_{failure}$ are calculated using as **Failure Criterion** a maximum Temperature close to Silicon temperature melting >= **1200K**
  - For each time pulse, the criterion has been applied in order to reconstruct the device behavior in terms of possible failure levels in the three regions (vfTLP, TLP and EOS)

Power – to – Failure: how to improve performances



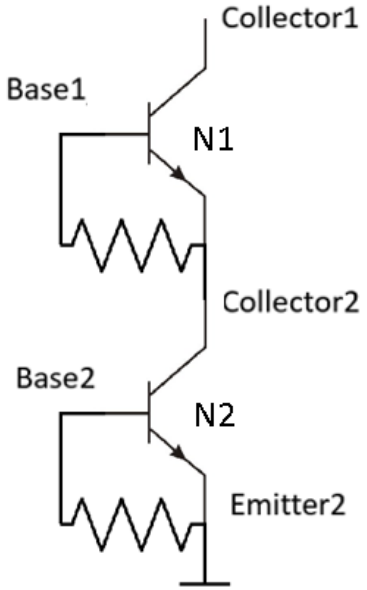




Conclusions

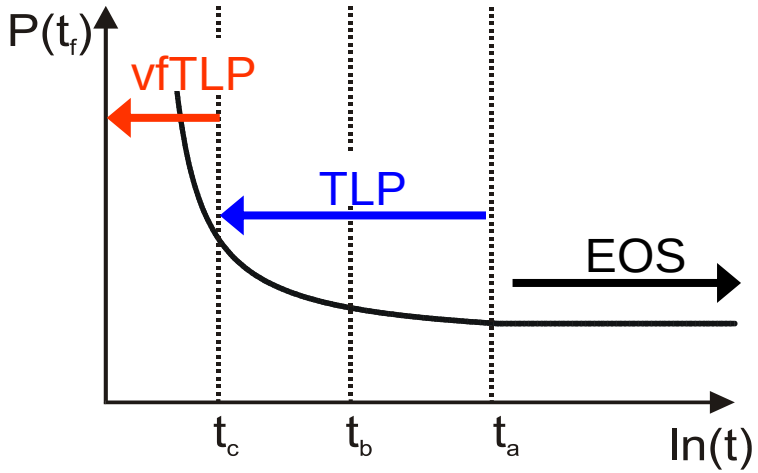
New technology:

Two low voltage BJTs to build an high voltage ESD protection



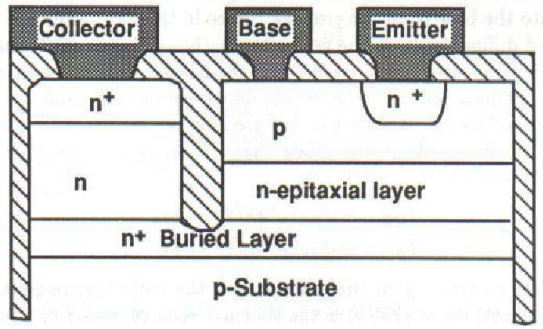
New Approach:

Temperature/Hot Spots failure criterion to predict very fast TLP stress performances

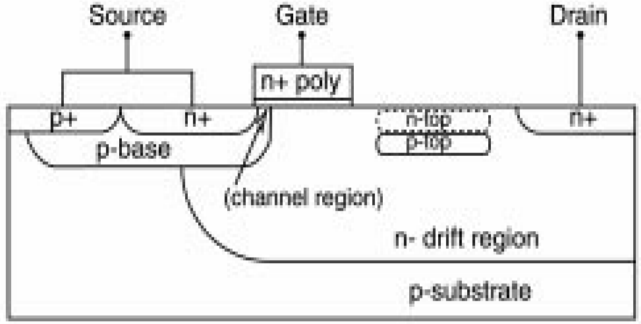


Future work:

Test the new approach in a different device based on LDMOS (planar double-diffused MOS) technology



BiCMOS technology



LDMOS technology

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- “Design and Analysis of an Area-Efficient High Holding Voltage ESD Protection Device” Jie Zeng, Shurong Dong, Senior Member, IEEE, Juin J. Liou, Fellow, IEEE, Yan Han, Lei Zhong, and Weihuai Wang, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 62, NO. 2, FEBRUARY 2015


thank you
danke
謝謝
ngiyabonga
teşekkür ederim
gracias
merci
obrigado
dziękuję
bedankt
спасибо
Баярлалаа
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grazie
terima kasih
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tapadh leat
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